Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.030”**

**.030”**

**T**

**A**

**C**

**For ZENER operation, Cathode must be operated positive with rewpect to Anode**

**Backside Potential: NOT CATHODE; must be electrically isolated**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: A = .0105” X .012”**

**C= .0055 X .022”**

**Mask Ref: CT6.2-O00**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 10/21/21**

**MFG: MICROSEMI / CDI THICKNESS .010” P/N: 1N827**

**DG 10.1.2**

#### Rev B, 7/19/02